

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
In re application of: Raminderpal Singh, et al.	Date: July 12, 2006
Serial Number: 10/807,478	Examiner: Stacy Whitmore
Filed: 3/23/2004	Group Art Unit: 2825
Title: Method of Checking the Layout Versus the Schematic of Multi-Fingered MOS Transistor Layouts Using a Sub-Circuit Based Extraction	IBM Corporation D/18G, B/321, Zip 482 2070 Route 52 Hopewell Junction, NY 12533-6531

AMENDMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Responsive to the Office Action dated April 19, 2006, the following Amendment is being submitted to place the above-identified application in prima facie condition for allowance.

Kindly amend the following claims and consider the following Remarks: